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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/724,663	11/28/2000	Jerome F. Duluk Jr.	A-66398-1/JAS	9392

7590 04/20/2005

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EXAMINER	
NGUYEN, HAU H	

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 04/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/724,663	DULUK JR. ET AL.	
	Examiner	Art Unit	
	Hau H Nguyen	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *1 and 5-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-4 and 16-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/03/01, 05/22/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 2, 3, and 16 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 15 and 31 of U.S. Patent No. 6,228,730. Although the conflicting claims are not identical, they are not patentably distinct from each other because the features of claims 2, 3, and 16 of the application are contained in claims 15 and 31 of U.S. Patent No. 6,228,730.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-4, 16-21, 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brayton et al. (U.S. Patent No. 5,623,628) in view of Cox et al. (U.S Patent No. 5,852,451).

Referring to claims 2-4, 16-21, Brayton et al. teach a method having a mechanism for ensuring consistency of data among various levels of caching. The cache consistency mechanism includes an external bus request queue which cooperate to monitor and control the issuance of data requests. As shown in Fig. 6, Brayton et al. teach the memory subsystem includes a memory order buffer (MOB) that controls dispatching within the memory subsystem (a memory control block). The memory order buffer comprises a load buffer 630 (a first order queue) and store buffer 631. These buffers handle all LOAD and STORE operations and track the progress of these operations as they move through the processor. When an operation is dispatched to and cannot complete due to an address or resource conflict, the MOB blocks the operation (stalling addresses) and stores the dependency information (col. 11, lines 33-42) (a conflict queue) (please see also col. 24, lines 49-58). As shown in Fig. 7, Brayton et al. teach the load buffer 710 is used to impose access ordering on memory loads. Each load operation is tagged with the stored buffer ID of the store previous to it (col. 14, lines 40-47) (an in-order tag queue). As shown in Fig. 14, Brayton et al. teach the conflict detector circuit 1472 accesses the inbound queue circuit 1474 and the in-order queue circuit 1470. The conflict detector circuit 1472 determines whether a

transaction logged in the in-order queue circuit 1470 is targeted for that same cache line a remote transaction logged in the inbound queue circuit 1474. The conflict detector circuit 1472 enters an invalidate line entry for a back invalidation transaction into the outbound queue circuit 1476 if the conflicting remote access to a cache line is detected. The back invalidation transaction is later issued over the bus 1430 to cause a retry of the conflicting access. The abort and redispatch process is illustrated in Fig. 15 (reassembling data in a specific order) (col. 30, lines 11-31).

Thus, Brayton et al. teach all the limitations of claims 2-21, except for coupling the reordered requests to a texture memory.

However, Cox et al. teach method of reordering memory references required to process independent pixels in a texture mapping system in order to achieve improved memory locality and hence improved graphics performance using conventional page-mode memory components (col. 3, lines 6-11), wherein a PPH (pixel priority heap) is employed to reorder addresses into texture memory to perform more reads from the same page before that page is closed and another opened or to reorder reads and writes from/to other clients as well. For example, PPH may be used to reorder references to destination addresses in the frame buffer to improve locality (col. 3, lines 31-42).

Therefore it would have been obvious to one skilled in the art to utilize the method as taught by Cox et al. in combination with the method as taught by Brayton et al. in order to allow the graphics rasterization engine to achieve better bandwidth using conventional page-mode memory components and without require extreme memory interleaving (col. 3, lines 25-30).

In regard to claims 25-27, as shown in Fig. 7, Cox et al. teach a flowchart of a PPH 202 read operation based on a two-cycle pipeline. The timing in this pipeline is based on two-phase

clocking. In the first phase, PPH 202 processes signals from storage through combinational logic. In the second phase, storage is updated. On cycle t, steps 700 through 704 occur; on cycle t+1, steps 705 through 707 occur. Cycle t: First, the signals from control module 304 to heap module 305 must be valid. Then heap module 305 generates 701 all o_pixel_status[ ] bits. MPE 303 selects 702 an index and provides it to control module 304 and pixels module 306. Control module 304 updates 703 last_bank, last_index, and bank[i_ index]. Pixels module 306 saves 704 the index obtained in 702 for use in the next cycle (saving the texel). Cycle t+1: The index of the entry in heap module 305 that was selected in 702 last cycle (if any) is written 705 to available module 301 (o_done_index). Pixels module 306 writes 706 the pixel at rindex (last cycle's i_index) to memory controller 204 (reusing the stored texel) (col. 12, lines 63-67, and col. 13, lines 1-15).

Therefore it would have been obvious to one skilled in the art to utilize the method as taught by Cox et al. in combination with the method as taught by Brayton et al. in order to allow the graphics rasterization engine to achieve better bandwidth using conventional page-mode memory components and without require extreme memory interleaving (col. 3, lines 25-30).

5. Claims 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brayton et al. (U.S. Patent No. 5,623,628) in view of Cox et al. (U.S Patent No. 5,852,451), and further in view of Papworth et al. (U.S. Patent No. 5,778,245).

Referring to claims 22-24, as cited above, Brayton et al. and Cox et al. teach all the limitations of claims 22-24, except that the texture memory comprises content addressable memory.

However, content addressable memory is well-known in the art as described in '245 to Papworth et al. Papworth et al. teach a method of reordering memory address, wherein as shown in Fig. 6, comprising MOB (memory order buffer) 503 responds to load operations by forwarding buffered data as necessary. When an operation is dispatched and cannot complete due to some address or resource conflict, MOB 503 blocks the operation and stores the dependency information. MOB 503 redispatches block operations when the blocking source is removed. MOB 503 controls the necessary monitoring and dispatched these non-speculative operations at the correct time. For instance, MOB 503 snoops the source addresses of instructions fetched and generates a single stall signal for the bus controller to stall an instruction fetch whenever the source address instruction being fetched substantially matches any of the addresses of the store destinations of the buffered stored instructions (col. 16, lines 15-32). Papworth et al. further teach a separate tag array 601 (Fig. 7), and the memory is implemented using content addressable memory as shown in Fig. 17.

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Papworth et al. in combination with the method as taught by Brayton et al. and Cox et al. in order to provide different allocation schemes to different resources in order to increase efficient use of the resource buffers, and also to allocate and deallocate instructions from the resources in an efficient manner (col. 2, lines 43-50).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 571-272-7787. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 571-272-7778.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9306 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (571)-272-2600.

H. Nguyen

04/18/2005

Matthew C. Bella

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600